Here, reference code 0B677h denotes a synchronization word for identifying the leading frame of the super frame, and is referred to as w2. Reference code F4988 denotes a synchronization word for identifying the second to eighth frames of the super frame, and is referred to as w3 being equal to logic reverse of w2. Accordingly, w2 is used as a superframe identifying signal showing the super frame leader formed by 8 frames. W3 is transmitted in the second to eighth frames in the superframe.

Insertion of the pseudo-data of the present invention is executed between w2/w3 and the subsequent TS data. In the present one embodiment, the pseudo-data will be all set to 0. However, data calculated in advance so as not to destroy convolution relationship in 12 symbols portion shifting from w2/w3 to the fixed data and 12 symbols portion shifting from the fixed data to the TS data will be inserted. These data here will be described as related fixed data.

Next, calculation method on these related fixed data will be described. For this, an encoder with industrial standards of constraint length k=7, and generator polynominal 171 and 133 (Octopal) to be ~~sued~~ used for convolution encoding and a parallel/serial converter to bring outputs C0 and C2 from this encoder with C0 as a leader into parallel/serial conversion are used.

For example, 0 data are added to all the tails of base data A340Ah or 5CBFh of the related fixed data subsequent to w2/w3 to generate w2/w3 for convolution encoding and parallel/serial conversion so that 000h or ~~268h~~ 26Bh subsequent to 0B677h or F4988h is generated.

symbol TMCC signal period, circuit sizes of the FIFO circuit 9 can be made to be the smallest. Accordingly, the necessary capacity of the FIFO circuit will be 48 symbols.

As described above, the pseudo-pattern generator 8 generates related fixed data of 96 symbols being QPSK-processed symbols. The rate is a transmission symbol rate and pseudo-pattern generator 8 starts generating the related fixed data from the rising edge of the selection signal SB to continue generating them during the period of higher voltage.

When the selection signal SB is at higher voltage, the selector 6B outputs the signal outputted from the pseudo-pattern generator 8 at the same time, and therefore an output from the selector 6B will be configured by bringing time-compressed TMCC signals and pseudo-patterns into time-division multiplex as shown in FIG. 3(F). In addition, into the selector 6, this base band signals Ia and Qa and the base band signals ID and QD which are produced by delaying the output of and the selector 6A with the delay circuit 11 are inputted and Ia and Qa are selected during the period when the selection signals S are with higher voltage to be outputted, and thereby the outputs Ib and ~~Qb~~ Qb of the selector 6 will be as shown in FIG. 3(H).

At this time, delay in the delay circuit 11 covers 96 symbols. In addition, in the selector 6A, when the selection signals SA are with higher voltage, the outputs IA and QA of the S/P converter 7 are selected to be outputted, but since the selection signals SA, which is set at higher voltage only during the main signal section to be transmitted at BPSK, r=1/2, is always set at lower voltage in the